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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,886	03/31/2004	Yoshikazu Ogawa	251311US2	4566

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
05/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/812,886	OGAWA	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The examiner acknowledges and accepts the amendments made to remedy the claim objections.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Postiff et al. (US PGPub 2003/0217249) in view of Witt et al. (US Patent 6,189,087).

4. As per claim 1:

Postiff teaches a processor having a register renaming function, comprising:

an instruction fetch part configured to fetch an instruction (Postiff: Figure 1, item 14);

a decoding part configured to decode an instruction code from the instruction fetched by the instruction fetch part (Postiff: Figure 1, item 16);

a register part configured to hold data corresponding to a register number indicated by the instruction code decoded by the decoding part (Postiff: Figure 1, item 12) (Please note that the register files are mislabeled in the drawings; the logical register file is item 12 and physical register file is item 10);

a caching register configured to cache the contents held by said register part (Postiff: Figure 1, item 10; paragraph 0027);

an inner instruction information holding part configured to hold information on a state of an inner instruction including a logical register number and a caching register number, which are held by said caching register by an instruction from said instruction fetch part (Postiff: Figure 4, item 50; paragraph 0035);

an instruction insertion determining part configured to compare an instruction code, with information on a state of the inner instruction, which is held by said inner instruction information holding part, to determine whether the inner instruction is to be inserted (Postiff: paragraph 0035); and

a register transfer instruction issuing part configured to issue a register transfer instruction for transferring inner data between said caching register and said register part when said instruction insertion determining part determines that the inner transfer instruction is to be inserted (Postiff: paragraph 0035) (The transfer between the source registers and the reservation stations),

thereby the processor having a register renaming function for sequentially rewriting the contents of a register alias table using a reorder buffer and a physical register free list, said reorder buffer holding a correspondence of a logical register number to its physical register number, which are included in the decoded instruction code, in a register alias table and storing an assignable number of the physical register number in the physical register free list to store a correspondence of an instruction

number, an architecture register number and an old physical register number (Postiff: paragraphs 0029-0033 and 0039).

Postiff does not teach the instruction code being obtained by pre-decoding the instruction from said instruction fetch part while Witt does (Witt: column 7, line 64 to column 8 line 16).

Witt states that CISC instructions in a superscalar processor can be inhibiting (Witt: column 1, line 41 to column 2, line 26). This is overcome by cracking instructions into smaller uOPs (ROPs). This cracking can also be time consuming, but Witt's method facilitates processor performance by ascertaining opcode and addressing information from the CISC instructions before they can be fully decoded (Witt: column 2, lines 30-41).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Witt's pre-decoding method would facilitate the processor performance of Postiff.

5. As per claim 2:

A processor having a register renaming function as set forth in claim 1, wherein said register part comprises a logical register capable of being referred on a program (Postiff: Figure 1, item 12), and said caching register comprises an inner register configured to hold a part of said logical register (Postiff: paragraph 0027), said register transfer instruction issuing part comprising a converting part for converting it into an inner register number, which is used by said logical register and said inner register, and a code producing part configured to produce a code in the same form as that of a

processor inner instruction code for transferring data between said logical register and said inner register (Postiff: paragraphs 0029-0038).

6. As per claim 3:

A processor having a register renaming function as set forth in claim 1, which further comprises a pre-decoding part configured to pre-decode an instruction from said instruction fetch part to an instruction code (Witt: column 7, line 64 to column 8 line 16).

7. As per claim 4:

A processor having a register renaming function as set forth in claim 3, wherein a register instruction inserting unit is configured to insert a load register instruction and a store resister instruction by said pre-decoding part, said instruction insertion determining part and said register transfer instruction issuing part, to issue an instruction (Witt: column 10, line 45 to column 11, line 11) (When cracking instructions, it is standard to replace a complex memory/memory instruction with several uOPs – load, load, exe, store. There must be logic present to be able to insert these load and store instructions).

8. As per claim 5:

A processor having a register renaming function as set forth in claim 4, wherein said register instruction insertion unit comprises:

an inner instruction holding part configured to hold said inner instruction information (Postiff: Figure 4, item 50);

a pre-decoding part configured to fetch register number information from an instruction code supplied from said instruction fetch part (Witt: column 7, line 64 to column 8, line 16);

an insertion instruction register number producing part as said instruction insertion determining part configured to compare said register number information, which is supplied from said pre-decoding part, with a logical register number, which is stored in a TAG region of the inner instruction information held by said inner instruction holding part, to produce a register number of an insertion instruction (Postiff: paragraphs 0029-0038); and

a load/store register instruction issuing part as said register transfer instruction issuing part configured to issue a load/store register instruction on the basis of the register number of said insertion instruction produced by the insertion instruction register number producing part (Witt: column 10, line 45 to column 11, line 11).

9. As per claim 6:

A processor having a register renaming function as set forth in claim 5, which further comprises an instruction insertion control part configured to add an instruction from said load/store register instruction issuing part before the instruction supplied from said instruction fetch part, to the added instruction to said instruction decoding part on the basis of said load/store register instruction issuing part, said instruction insertion control part being provided between said instruction fetch part and said instruction decoding part (Witt: column 10, line 45 to column 11, line 11).

10. As per claims 7-16:

Claims 7-16 recite the same limitations as claims 1-6 and are rejected for the same reasons.

Response to Arguments

11. Applicant's arguments filed 3/9/07 have been fully considered but they are not persuasive.

12. The applicant has made the following argument:

> "First, applicants submit Witt does not cure the recognized deficiencies in Postiff as Witt does not disclose or suggest the 'instruction code being obtained by pre-decoding the instruction from said instruction fetch part'."

While the examiner recognizes that Witt discloses a "predecode" operation earlier than the cited portion, the examiner used the citation of Witt: column 7, line 64 to column 8 line 16 because the examiner has taken the position of DECODE1 to be a predecode operation. "Predecode" is a vague term in the art that could mean numerous things. The prefix "pre" simply means preceeding, or before. Therefore a predecode is any action that takes place before an actual decode is done, since the actual decoding is done in DECODE2, DECODE 1 represents a predecode operation.

13. The applicant has made the following argument:

> "Applicants submit that disclosure in Postiff does not correspond to the 'register transfer instruction issuing part' in the claims. Specifically that disclosure in Postiff does not indicate any transfer of inner data between a caching register (for example element 3 in Figure 1, element 300 in Figure 2) and a register part (for example element 4 in Figure 1, element 400 in Figure 2) based on determining that an inner transfer instruction is to be inserted."

The act of data forwarding based on register rename constitutes a black box internal mechanism that completes the action of a 'register transfer instruction issuing

part'. The register part is the source operand and the caching register is the reservation station registers.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER